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SYSTEM AND METHOD FOR DATA PHASE REALIGNMENT

Abstract

A system and method for aligning data transferred across circuit boundaries having different clock domains. The system includes a buffer circuit comprising a latch for receiving data clocked in a first clock domain and latching the received data in a second clock domain by one of a first edge of a second clock signal, or a second opposite edge of the second clock signal. The first and second clock signals are of the same frequency but operating out of phase. A control circuit receives the first and second clock signals and determines a phase relationship therebetween. The control circuit generates a control signal based on the determined phase relationship which is implemented for selecting one of a rising edge of the second clock signal, or a falling edge of the second clock signal, for latching action in the second clock domain. Reliable data transfer operation is provided for all possible phase relationships of the first and second clock signals.